The following Listing of Claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

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1. (Currently Amended) A method for making a dielectric structure for dual-damascene applications, the method comprising:

providing a substrate;

fabricating metallization lines within the substrate;

forming a barrier layer over the metallization lines and the substrate;

forming an inorganic dielectric layer to define a via dielectric layer directly over the barrier layer, the inorganic dielectric layer having a dielectric constant of about 4 and being highly selective relative to the barrier layer when etched; and

forming a carbon doped oxide layer to define a trench dielectric layer over and in direct contact with the inorganic dielectric layer, the trench layer being formed to define a metallization line layer.

2. (Previously Presented) A method for making a dielectric structure for dual-damascene applications as recited in claim 1, further comprising:

forming a trench in the carbon doped oxide layer using a first etch chemistry.

3. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 2, further comprising:

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forming a via in the inorganic dielectric layer using a second etch chemistry, the second etch chemistry being different than the first etch chemistry and the via being within the trench.

4. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 1, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

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5. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 4, wherein the forming of the inorganic dielectric layer includes,

depositing a TEOS silicon dioxide material over the barrier layer.

6. (Previously Presented) A method for making a dielectric structure for dual-damascene applications as recited in claim 5, wherein the carbon doped oxide layer is a low dielectric constant layer having a dielectric constant of about and no greater than 3.0.

7. (Previously Presented) A method for making a dielectric structure for dual-damascene applications as recited in claim 3, wherein the inorganic dielectric layer is one of a TEOS oxide layer and a fluorine doped oxide layer.

8. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 7, wherein the first etch chemistry is optimized to etch through the

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carbon doped oxide layer and the second etch chemistry is optimized to etch through the TEOS oxide layer or the fluorine doped oxide layer.

9. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 8, wherein the second etch chemistry is selective to the barrier layer.

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10. (Currently Amended) A method for making a multi-layer inter-metal dielectric over a substrate, comprising:

forming a barrier layer over the substrate;

forming a silicon dioxide layer over the barrier layer, the silicon dioxide layer having a dielectric constant of about 4;

forming a carbon doped oxide layer directly over and in direct contact with the silicon dioxide layer;

forming a trench through the carbon doped oxide layer; and

forming a via in the trench extending through the silicon dioxide layer to the barrier layer,

wherein the silicon dioxide layer defines a via layer and the carbon doped oxide layer defines a trench layer for metallization lines.

11. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

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12. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 11, wherein the forming of the silicon dioxide layer includes,

depositing one of an un-doped TEOS oxide layer and a fluorine doped oxide layer.

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13. (Previously Presented) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 12, wherein the carbon doped oxide layer is a low dielectric constant layer having a dielectric constant less than or equal to about 3.0.

14. (Previously Presented) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein forming the via in the trench extending to the barrier layer further includes,

implementing a first chemistry optimized to etch through the carbon doped oxide layer; and

implementing a second chemistry which is different than the first etch chemistry and is optimized to etch through the silicon dioxide layer.

15. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 14, wherein the second chemistry that is optimized to etch through the silicon dioxide layer is selective to the barrier layer.

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16. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 15, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

17-25. (Canceled)

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26. (Original) A method for making a multi-layer intermetal dielectric over a substrate as recited in claim 10, further comprising:

etching the barrier layer; and

forming a via and trench barrier layer to cover a surface within the via and the trench,

wherein the via and trench barrier layer is one of tantalum nitride material and tantalum material.

27. (Withdrawn) A method for fabricating a multi-layer inter-metal dielectric semiconductor structure, comprising:

providing a base dielectric layer;

fabricating metallization lines within the base dielectric layer by etching and filling with metallization;

depositing a barrier over the metallization lines and the base dielectric layer;

depositing an inorganic dielectric layer over the barrier;

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depositing a low dielectric constant (low K) layer over the inorganic dielectric layer, wherein a thickness of the low dielectric constant layer is greater than a thickness of the inorganic dielectric layer;

etching a trench in the low dielectric constant layer using a first etch chemistry, the etching being timed to etch through a partial thickness of the low dielectric constant layer, and wherein the first etch chemistry is optimized to a selected low dielectric constant material;

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defining locations of via holes in the trench with a photoresist mask;

etching the via holes through a remaining thickness of the low dielectric constant layer using the first etch chemistry;

etching the via holes through the inorganic dielectric layer to the barrier using a second etch chemistry, the second etch chemistry being highly selective to the barrier;

removing the barrier from a region in the via hole over a metallization line;

forming a barrier layer in the trench and via holes; and

filling the trench and via holes with metal.

28. (Withdrawn) A method for fabricating a multi-layer inter-metal dielectric semiconductor structure as recited in claim 27, wherein the inorganic dielectric layer is one of TEOS dielectric material and fluorine doped dielectric material, and the low dielectric constant layer is carbon doped oxide.

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29. (Withdrawn) A method for fabricating a multi-layer inter-metal dielectric semiconductor structure as recited in claim 27, wherein the first etch chemistry is one of $Ar/O_2/CF_4$, $Ar/CO/CF_4/C_4F_8$, $Ar/O_2/C_4F_8$, $N_2/O_2/C_2H_2F_4$, $N_2/O_2/C_2H_4$, $H_2/CF_4/Ar$, and Cl_2/O_2.

30. (Withdrawn) A method for fabricating a multi-layer inter-metal dielectric semiconductor structure as recited in claim 27, wherein the second etch chemistry is $C_4F_8/CO/Ar/O_2$.

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31. (Withdrawn) A method for fabricating a multi-layer inter-metal dielectric semiconductor structure as recited in claim 27, wherein the thickness of the inorganic dielectric layer is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer and the inorganic dielectric layer is about 10,000 Angstroms.